CUSTOMER STORY

ACCELERATING DESIGN FOR VLSI

REDUCING REGRESSION TESTING TURNAROUND TIME WITH BETTER RESOURCE MANAGEMENT

About the Customer

CEVA is the leading licensor of wireless connectivity and smart sensing technologies. CEVA's ultra-low-power IPs include comprehensive DSP-based platforms for 5G baseband processing in mobile and infrastructure, AI processors for neural network workloads, advanced imaging and computer vision for any camera-enabled device and audio/voice/speech and ultra-low power always-on/sensing applications for multiple IoT markets. More than 12 billion CEVA-powered chips have been shipped worldwide, for a wide range of diverse end markets.

CEVA has been using Altair Accelerator™ technology for years for managing engineering resources and speeding VLSI development flows.

> "Current DSP IPs have many verification challenges; it's essential that we use every available simulation cycle during the design phase. That means 100% utilization of both compute hardware and simulation software licenses."
>
> Noam Meser, Director of VLSI Verification and Infrastructure, CEVA

Their Challenge

As an IP design and licensing company, time-to-market and engineering efficiency are CEVA's most critical and valued metrics. With this in mind, the team at CEVA selected the Altair Accelerator™ job scheduler for their VLSI workflows.

The challenge is allowing the engineering team to work as if they have no constraints, enabling easy access to HW compute servers, EDA licenses, and automated design flows without exceeding a project's R&D budget.

Our Solution

Altair Accelerator is designed to saturate resources while allowing time-critical jobs to start executing immediately. A key element in optimizing resource usage is the ability to monitor the state of the job queue and resource availability. Accelerator's single queue model enables all design engineers to see their jobs in the context of others and to understand why a particular job is waiting. The clarity enables design teams to self-regulate and to choose the best approach for sharing critical resources. While these human factors are important, Accelerator has a number of techniques for continuous optimization, notably preemption and license-to-job matching.

With preemption, Accelerator is able to detect that time-critical jobs are waiting and make immediate adjustments to running jobs with either a suspension of a withdrawal or resubmit.

Noam Meser, Director of VLSI Verification and Infrastructure at CEVA says: "We were able to build an advanced suspend-resume mechanism based on the Accelerator's preemption feature which enables full utilization of simulation licenses and 24/7 regressions without harming the fluent work of daily users that could now run their jobs by suspending and later resuming a low prioritized regression."

Accelerator's preemption system is rule-based which allows CEVA to modify policies as needed. Further, license-to-job matching allows a job's license utilization to be profiled along RAM & CPU usage. Collecting this information over time allows the management team to optimize future spend in these resources.

Results

Accelerator allows CEVA engineers to get the most from the available resources in a manner that suits their design approach. Licenses utilization is constantly at 100%, automating new jobs dispatches according to the flow policy.

Software (tool licenses) and hardware (compute hosts) constraints are managed with confidence and care using close monitoring, historical statistics, and defined workflow policies.
Multiple VLSI projects are being completed successfully and on time.
CEVA keeps tight control on costs and benefits with a detailed view into resource usage by projects and users.

Altair Accelerator brings over 25 years of experience with leading VLSI companies in Silicon Valley and worldwide to empower the CEVA team to validate and enrich their implementation of the Accelerator technology.

To learn more, please visit altair.com/accelerator